Claim 1 is rejected under 35 U.S.C. § 102 for anticipation based upon Hasegawa, JP 6-50824

In the third enumerated paragraph of the Office Action, the Examiner asserted that Lee discloses a semiconductor device corresponding to that claimed. This rejection is respectfully traversed.

In the Amendment filed August 19, 2003, Applicant amended claim 1 to include the limitations of claim 8, which directly depended from claim 1. In the Office Action dated May 20, 2003, the Examiner indicated that claim 8 is allowed. However, the Examiner apparently views the teachings of Hasegawa differently since claim 1 is still rejected under 35 U.S.C. § 102 for anticipation based upon Hasegawa. With regard to the limitation previously presented in claim 8 (i.e., electromigration arises in the second interconnection when a predetermined voltage is applied to the second interconnection, thereby establishing connection between the second interconnection and a plug), the Examiner stated the following:

> when a predetermined voltage is applied to said second interconnection, electromigration **could** arise in said second interconnection capable of establishing connection between said second interconnection and said plug (emphasis added).

The factual determination of anticipation under 35 U.S.C. § 102 requires the identical disclosure of each element of a claimed invention in a single reference. As part of this analysis, the Examiner must (a) identify the elements of the claims, (b) determine the meaning of the elements in light of the specification and prosecution history, and (c) identify corresponding elements disclosed in the allegedly anticipating reference. If the Examiner cannot identically disclose each element of the claimed invention, the Examiner can establish anticipation under 35 U.S.C. § 102 by establishing that the element not explicitly disclosed is inherently disclosed by the applied prior art. The Examiner, however, has failed to do either.

Initially, Applicant notes that the Examiner neither clearly designated the teachings in Hasegawa being relied upon to teach the limitations discussed above nor clearly explained the pertinence of Hasegawa in teaching these limitations. Thus, the Examiner has failed to establish that Hasegawa explicitly discloses these limitations. In this regard, the Examiner's rejection under 35 U.S.C. § 102 also fails to comply with 37 C.F.R. § 1.104(c).[1] Not only has the Examiner failed to establish that Hasegawa explicitly discloses these limitations, the Examiner has failed to establish that these limitations are inherently disclosed by Hasegawa.

Inherency may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient to establish inherency.[2] To establish inherency, the extrinsic evidence must make clear that the missing element must necessarily be present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.[3] Furthermore, as articulated by the Honorable Board of Patent Appeals and Interferences in ex parte Schricker, 56 USPQ2d 1723, 1725 (BPAI 2000):

> However, when an examiner relies on inherency, it is incumbent on the examiner to point to the "page and line" of the prior art which justifies an inherency theory. Compare, In re Rijckaert, 9 F.3d 1531, 1533, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (when the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the prior art); In re Yates, 663 F.2d 1054, 107, 211 USPQ 1149, 1151 (CCPA 1981).

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[1] 37 C.F.R. § 1.104(c) provides:

> In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

[2] In re Rijckaert, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); In re Oelrich, 666 F.2d 578, 212 USPQ 323, (CCPA 1981).

[3] Finnegan Corp. v. ITC, 180 F.3d 1354, 51 USPQ2d 1001 (Fed. Cir. 1999); In re Robertson, 169 F.3d 743, 49 USPQ2d 1949 (Fed. Cir. 1999); Continental Can Co. USA v. Monsanto Co., 20 USPQ 2d 1746 (Fed. Cir. 1991); Ex parte Levy, 17 USPQ2d 1461 (BPAI 1990).

By asserting that the feature discussed above "could arise" in Hasegawa, the Examiner has admitted that this feature does not necessarily arise from the teachings of Hasegawa. Therefore, the Examiner has not established that this limitation is inherently disclosed by Hasegawa. The Examiner is also referred to M.P.E.P. § 2112, entitled "Requirements of Rejection Based on Inherency; Burden of Proof." Applicant, therefore, respectfully submits that the imposed rejection of claim 1 under 35 U.S.C. § 102 for anticipation based upon Hasegawa is not factually viable and, hence, solicit withdrawal thereof.

Not only does Hasegawa fail to identically disclose the claimed invention as recited in claim 1, one having ordinary skill in the art would not have been motivated to modify Hasegawa so as to arrive at the claimed invention. Hasegawa's device is capacitor that acts as a temperature sensor. As stated in the English-language Abstract of Hasegawa, "[a] change of the gap (g) due to temperature is measured as a change in capacitance or tunnel current and thereby the temperature is detected." If Hasegawa were modified such that a connection was established between the asserted second connection (i.e., feature 24) and the asserted plug (i.e., feature 26), as recited in claim 1, Hasegawa would cease to operate, as intended, since this structure would no longer act as a capacitor. In this regard, it has been repeatedly held that one having ordinary skill in the art cannot be presumed realistically motivated to modify a reference in the manner inconsistent with the disclosed objectives, which in the case of Hasegawa, is to provide a capacitive structure that measures temperature.

Claims 2-5 are rejected under 35 U.S.C. § 103 for obviousness based upon Hasegawa in view of Jain et al., U.S. Patent No. 6,107,165

In the fifth enumerated paragraph of the Office Action, the Examiner concluded that one having ordinary skill in the art would have been motivated to modify the semiconductor device of Hasegawa in view of Jain to arrive at the claimed invention. This rejection is respectfully traversed.

With regard to claims 2-5, the Examiner stated the following:

> As to the formation of the said void by various means recited in claims 2-5, "product by process" claims are directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685 and In re Thorpe, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

The Examiner statement of the law regarding "product by process" limitations is not only incomplete and misleading, the Examiner's statement is also partly erroneous. The case law is clear that a product-by-process limitation must be considered by the Examiner in making a determination of novelty or obviousness. Although the Examiner has a reduced burden of proof with regard to product-by-process claims, as discussed in M.P.E.P. § 2113, the Examiner must first provide a rationale to show that the claimed product and prior art products actually do appear to be identical or substantially identical.

The Examiner, however, has failed to make any reasoned argument as to why the claimed void, which is formed by removal of a barrier layer, is identical or substantially identical to the void of Hasegawa. Therefore, the Examiner has failed to meet the requirements established by case law and M.P.E.P. § 2113 regarding product-by-process limitations.

Notwithstanding the Examiner's failure to consider the product-by-process limitations recited in the claims, the recited product-by-process limitations result in a structural difference between the claimed invention and the semiconductor device disclosed by the applied prior art. Specifically, both claims 2 and 4 recite that the void is formed by means of removing the barrier metal layer formed on the plug. Therefore, at least a portion of the barrier metal layer that would normally be disposed above the plug is removed. In contrast, Fig. 18 of Jain discloses that a complete barrier metal layer 27 is formed over the plug, and nowhere does Jain teach or suggest that a portion of that barrier metal layer 27 is removed to form a void.

Furthermore, *even if* the barrier metal layer 27 of Jain were removed, as recited in the claims, the claimed invention would not result. Both claims 2 and 4 recite that the predetermined void is between and separates the plug from the second interconnection. However, three different layers 20, 21 and 26 are between the barrier metal layer 27 and the plug 12 of Jain. Thus, even if a void were created by removing a portion of the metal layer 27, such a void would not be between and separate the plug 12 from the interconnection 27/28 of Jain, as recited in claims 2 and 4. Applicant, therefore, submits that the imposed rejection of claims 2-4 under 35 U.S.C. § 103 for obviousness based upon Hasegawa in view of Jain is not viable and, hence, solicits withdrawal thereof.

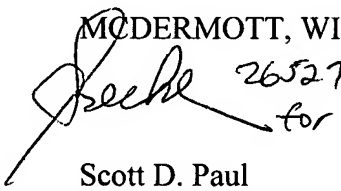
Applicant has made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicant invites the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing

remarks, Applicant hereby respectfully requests reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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